2) Amendments to the Claims

Claim 1 (amended): A method of patterning metal layers of a semiconductor wafer, the method comprising:

depositing a first conductive layer over a substrate;

depositing an insulating layer over the first conductive layer;

depositing a second conductive layer over the insulating layer;

depositing a first resist over the second conductive layer;

patterning the first resist with a first pattern;

depositing a second resist over the first resist;

~~patterning the first resist with a first pattern and~~ patterning the second resist with a second pattern; and

A1 simultaneously transferring the first pattern to the first conductive layer and the second pattern to the second conductive layer.

Claim 2 (original): The method according to Claim 1 wherein transferring the first and second patterns comprise exposing the wafer to a single reactive ion etch process.

Claim 3 (original): The method according to Claim 1 wherein the first resist comprises a negative resist and the second resist comprises a positive resist.

Claim 4 (original): The method according to Claim 1 wherein the first resist comprises a positive resist and the second resist comprises a negative resist.

Claim 5 (original): The method according to Claim 1 wherein the insulating layer comprises a capacitor dielectric, wherein transferring the first pattern to the first conductive layer comprises forming bottom metal plates of a MIM capacitor, and wherein transferring the second pattern to the second conductive layer comprises forming top metal plates of the MIM capacitor.

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Claim 6 (original): The method according to Claim 1 further comprising transferring the first pattern to the insulating layer.

Claim 7 (original): A method of patterning metal layers of a semiconductor wafer, the wafer comprising a first conductive layer, an insulating layer disposed over the first conductive layer and a second conductive layer disposed over the insulating layer, the method comprising:

depositing a first resist over the second conductive layer;

patterning the first resist with a first pattern;

depositing a second resist over the first resist;

patterning the second resist with a second pattern;

simultaneously transferring the first pattern to the first conductive layer and transferring the second pattern to the second conductive layer.

A1 cont

Claim 8 (original): The method according to Claim 7 wherein transferring the first and second patterns comprise exposing the wafer to a reactive ion etch process.

Claim 9 (original): The method according to Claim 8 wherein the first resist comprises a negative resist and the second resist comprises a positive resist.

Claim 10 (original): The method according to Claim 8 wherein the first resist comprises a positive resist and the second resist comprises a negative resist.

Claim 11 (original): The method according to Claim 8 wherein the insulating layer comprises a capacitor dielectric, wherein transferring the first pattern to the first conductive layer comprises forming bottom metal plates of a MIM capacitor, and wherein transferring the second pattern to the second conductive layer comprises forming top metal plates of the MIM capacitor.

Claim 12 (original): The method according to Claim 7 further comprising transferring the first pattern to the insulating layer.

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Claim 13 (amended): A method of forming capacitive plates of a MIM capacitor, comprising:

providing a wafer having a substrate;

depositing a first conductive layer on the substrate;

depositing a capacitor dielectric layer over the first conductive layer;

depositing a second conductive layer over the capacitor dielectric layer;

depositing a first resist over the second conductive layer;

patterning the first resist with a first pattern;

depositing a second resist over the first resist;

patterning the second resist with a second pattern; and

simultaneously transferring the first pattern to the first conductive layer and transferring the second pattern to the second conductive layer.

Claim 14 (original): The method according to Claim 13 wherein transferring the first and second patterns comprise exposing the wafer to a reactive ion etch process.

Claim 15 (original): The method according to Claim 13 wherein the first resist comprises a negative resist and the second resist comprises a positive resist.

A1 Claim 16 (original): The method according to Claim 13 wherein the first resist comprises a positive resist and the second resist comprises a negative resist.

Claim 17 (original): The method according to Claim 13 further comprising transferring the first pattern to the insulating layer.